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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,516	01/11/2002	Johann Fuhrmann	DE 01007	8286

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EXAMINER	
HU, SHOUXIANG	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/043,516	FUHRMANN ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show where is the chip in the chip card mentioned in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). In this case, the position of the chip, along with its relationships with the recited integrated circuit (which are formed on the carrier substrate, as defined in the claims) are essential for a proper understanding of the disclosed invention, as the disclosed invention's main objectives apparently is to protect the functions of the chip card.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 1-21 are objected to because of the following informalities and/or defects:

In claim 1, the term of "the two contact terminals" recited in line 9 lacks a sufficient antecedent basis in the claim.

In claim 1, line 10, the term of "of which unit" should read as: --of said signal-generating unit (40)--.

In claim 1, line 11, the term of "evaluation unit" should read as: --evaluation unit (7)--.

Claim 12 re-defines a set of capacitor, circuit units (including 40, 70, 55, 60) and a counting period, but fails to clarify what are the respective relationships between them and the corresponding ones already defined in claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Newly amended claims 1 and 12 each recite the subject mater that "the signal-generating unit (40) and the evaluation unit (70) are integral parts of the integrated circuit". However, the original disclosure lacks an adequate description regarding how and where the recited signal-generating unit (40) and evaluation unit (70) are formed so as to become integral parts of the recited integrate circuit. In claim 1, the recited integrated circuit is defined as being "constituted by at least two spaced conductor

tracks on the carrier substrate. And, according to the specification and the drawings, the signal-generating unit (40) and evaluation unit (70) have clear interface(s) with the recited spaced-track integrated circuit (20-27), instead of being integral parts of the recited spaced-track integrated circuit. According to the original specification (see the bottom paragraph on page 4), the signal-generating unit (40) and evaluation unit (70) of the recited circuit arrangement are integrated in the chip or smart card. However, it is not clear where the signal-generating unit (40) and evaluation unit (70) are formed (in the chip or in the recited carrier substrate or in other substrate?), and what are the positional relationships between the to-be-protected chip and the recited capacitor.

Furthermore, the claimed invention, especially the one in claims 19 and 21, defines that the functions of the integrated circuit can be blocked, locked, and/or interrupted. However, the specification lacks an adequate description regarding what are the recited functions of the spaced-track integrated circuit and how they are blocked, locked, and/or interrupted. According to the original specification, it appears that it is the function of the chip card or smart card that is intended to be protected through being blocked, locked, and/or interrupted.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 and 6-21, insofar as being in compliance with 35 U.S.C. 112 and as being best understood in view of the claim objections, are rejected under 35 U.S.C. 102(b) as being anticipated by Hierold et al. ("Hierold"; DE 19738990A1; of record).

Hierold discloses an electric or electronic circuit arrangement and a method of protecting a electronic circuit arrangement thereof (Figs. 1, 2, 5 and 7, particularly Fig. 5), comprising: a layered carrier substrate (2) of a semiconducting or insulating material; at least one integrated circuit constituted by at least two spaced and lithographically applied conductor tracks (20_1, see Fig. 5 in view of Fig. 1) on the carrier substrate (2); at least one dielectric shielding layer (all insulating layers above the substrate 2) including an inherent insulation layer and/or passivation layer (the layer between the substrate 2 and the layer 40) and/or a further protective layer (the insulating layer(s) above the layer 40) situated between the conductor tracks (20_1) and/or laterally with respect to the conductor tracks (20_1) and/or on the conductor tracks (20_1), provided for protecting the integrated circuit from external influences so that the integrated circuit has a specific, particularly lateral and/or particularly parasitic capacitance (C) determined by the dielectric shielding layer, characterized in that at least one signal-generating unit (51) including at least an oscillator unit is connected to the contact terminals (see Fig. 5) of the integrated circuit, the output frequency (f) of which unit is substantially determined by the specific capacitance, in that the signal-generating unit (51) precedes at least a first counting unit (521) which is clocked at the output frequency (f) of the signal-generating unit (51), in which counting unit an actual value count can be determined

after a predetermined temporal counting period, in that at least a second counting unit (53) clocked at a reference frequency is provided, in which counting unit a nominal value count can be determined after the predetermined temporal counting period, in that the first counting unit (51) and the second counting unit (53) precede at least one comparator unit (54) for comparing the actual value count with the nominal value count, while the functions of the integrated circuit can be blocked and/or locked and/or interrupted temporarily or permanently in the case of an error indication which occurs when the actual value count is compared with the nominal value count. In addition, it is noted that the signal-generating unit (40) and the evaluation unit (70) in Hierold are packed in unit 5 (see Fig. 7), which in turn is integrated with the integrated circuit constituted by the two spaced and lithographically applied conductor tracks (see Figs. 2, 4, and 5).

Regarding claim 2, the conductor tracks (20_1) in Hierold are at least sectionally arranged parallel to each other and/or in a meandering intermeshing configuration (see Fig. 5).

Regarding claims 6 and 20, it is noted that the signal-generating unit (51) in Hierold includes an oscillator, which normally inherently comprises at least one oscillator circuit consisting of at least one capacitive unit including a capacitor, and at least one resistive unit including a resistor, and/or at least one oscillator circuit consisting of at least one capacitive unit including a capacitor, and at least one inductive unit including a coil.

Regarding claims 7 and 13, a differential evaluation unit is naturally constituted by the first counting unit, the second counting unit and the comparator unit in Hierold.

Regarding claim 10, the arrangement in Hierold further includes a coding unit (522), which manifests that the first counting unit and/or the second counting unit are/is naturally formed on a digital basis.

Regarding claim 11, the arrangement of Hierold is for a chip card or smart card.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-5, as being best understood in view of the above claim objections, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hierold et al. ("Hierold"; DE 19738990A1; of record).

The disclosure of Hierold is discussed as applied to claims 1, 2 and 6-15 above.

Regarding claim 3, it is noted that the mutual distance between the conductor tracks is in an art-recognized result-effective parameter of importance subject to routine experimentation and optimization; and that the recited micrometer range is well with the art-recognized normal range for the mutual distance between capacitor electrodes.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the circuit arrangement of Hierold with the

distance between the conductor tracks being in the micrometer range, so that a circuit arrangement with optimized performance would be obtained, because it has been held that "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Regarding claims 4 and 5, it is noted that silicon oxide and opaque resin are each among art-recognized insulating passivation materials commonly used for reliably and/or invisibly protecting IC devices, as evidenced in the prior art such as Daum (US 5,821,582; see col. 3, lines 32-33) and/or Ban et al. (Us 6,060,773; see col. 1, lines 22-24).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the circuit arrangement of Hierold with the dielectric shielding layer being formed of silicon oxide or opaque resin, so that an IC device with reliable and/or invisible protection would be obtained.

Response to Arguments

6. Applicant's arguments filed on 12/20/03 have been fully considered but they are not persuasive.

Applicant's main arguments include that the applied prior art reference fails to teach the claimed subject matter that "the signal-generating unit (40) and the evaluation unit (70) are integral parts of the integrated circuit". However, as explained in the claim rejections under 35 U.S.C 112 set forth above in this Office action, such subject matter

is not fully supported by the original disclosure. Detailed responses to the arguments are fully incorporated into the claim rejections and claim objections set forth above in this Office action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
April 15, 2004

SHOUXIANG HU
PRIMARY EXAMINER